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# DATA SHEET

# BLF348
## VHF linear push-pull power MOS transistor

Product specification

October 1992

Philips Semiconductors

PHILIPS

# VHF linear push-pull power MOS transistor BLF348

## FEATURES

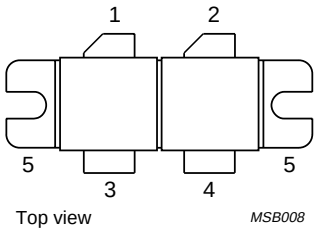
- High power gain
- Easy power control
- Good thermal stability
- Gold metallization ensures excellent reliability.

## DESCRIPTION

Dual push-pull silicon N-channel enhancement mode vertical D-MOS transistor, designed for broadcast transmitter applications in the VHF frequency range.

The transistor is encapsulated in a 4-lead, SOT262 A1 balanced flange envelope, with two ceramic caps. The mounting flange provides the common source connection for the transistors.

## PIN CONFIGURATION



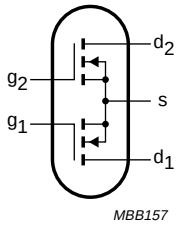




Fig.1 Simplified outline and symbol.

## CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static charge during transport and handling.

## PINNING – SOT262A1

| PIN | DESCRIPTION |
|---|---|
| 1 | drain 1 |
| 2 | drain 2 |
| 3 | gate 1 |
| 4 | gate 2 |
| 5 | source |

## WARNING

**Product and environment safety - toxic materials**

This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

## QUICK REFERENCE DATA

RF performance in a push-pull common source test circuit.

| MODE OF OPERATION | $f_{vision}$ (MHz) | $V_{DS}$ (V) | $I_D$ (A) | $T_h$ (°C) | $d_{im}$ (dB) (note 1) | $P_{o\ sync}$ (W) | $G_p$ (dB) |
|---|---|---|---|---|---|---|---|
| class-A | 224.25 | 28 | $2 \times 4.6$ | 70 | –52 | > 67 | > 11 |
| | 224.25 | 28 | $2 \times 4.6$ | 25 | –52 | typ. 75 | typ. 13 |

**Note**

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak synchronization level.

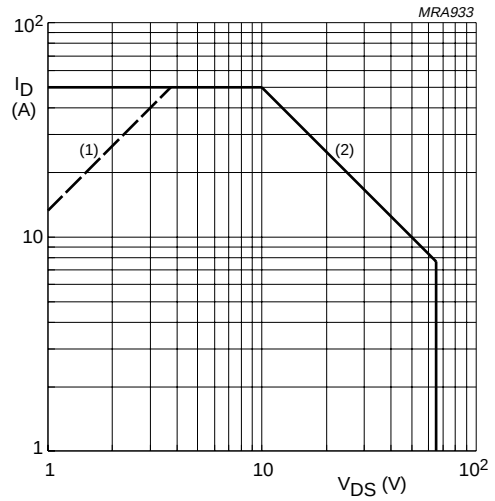
## LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).
Per transistor section unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{DSS}$ | drain-source voltage | | – | 65 | V |
| $\pm V_{GSS}$ | gate-source voltage | | – | 20 | V |
| $I_D$ | DC drain current | | – | 25 | A |
| $P_{tot}$ | total power dissipation | up to $T_{mb}$ = 25 °C; total device; both sections equally loaded | – | 500 | W |
| $T_{stg}$ | storage temperature | | –65 | 150 | °C |
| $T_j$ | junction temperature | | – | 200 | °C |

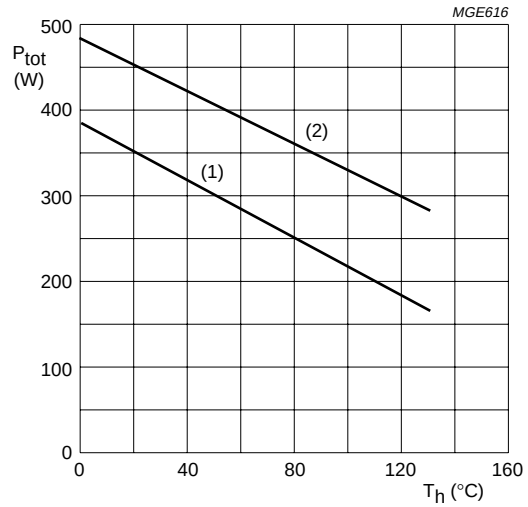
## THERMAL RESISTANCE

| SYMBOL | PARAMETER | CONDITIONS | THERMAL RESISTANCE |
|---|---|---|---|
| $R_{th\ j\text{-}mb}$ | thermal resistance from junction to mounting base | total device; both sections equally loaded | 0.35 K/W |
| $R_{th\ mb\text{-}h}$ | thermal resistance from mounting base to heatsink | total device; both sections equally loaded | 0.15 K/W |




(1) Current is this area may be limited by $R_{DS(on)}$.
(2) $T_{mb}$ = 25 °C.
Total device; both sections equally loaded.

Fig.2 DC SOAR.



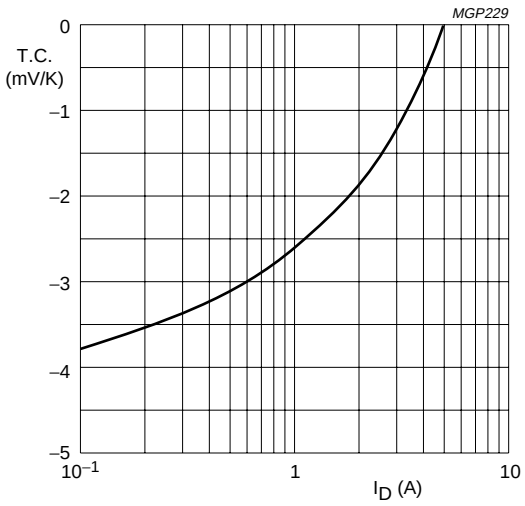

(1) Continuous operation.
(2) Short-time operation during mismatch.
Total device; both sections equally loaded.

Fig.3 Power/temperature derating curves.

**CHARACTERISTICS (per section)**

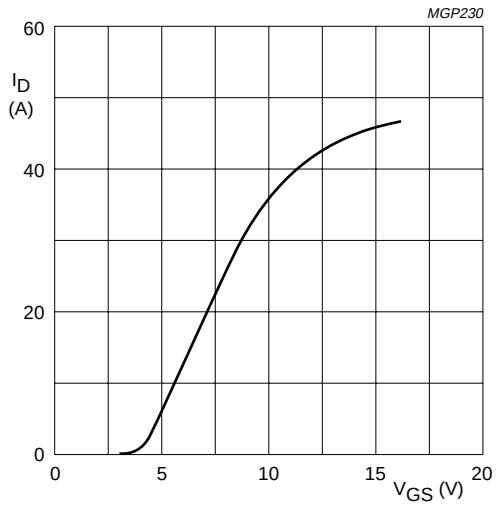
$T_j$ = 25 °C unless otherwise specified.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0; $I_D$ = 0.1 A | 65 | – | – | V |
| $I_{DSS}$ | drain-source leakage current | $V_{GS}$ = 0; $V_{DS}$ = 28 V | – | – | 5 | mA |
| $I_{GSS}$ | gate-source leakage current | ±$V_{GS}$ = 20 V; $V_{DS}$ = 0 | – | – | 1 | μA |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 0.1 A; $V_{DS}$ = 10 V | 2 | – | 4.5 | V |
| $\Delta V_{GS(th)}$ | gate-source voltage difference of both transistor sections | $I_D$ = 0.1 A; $V_{DS}$ = 10 V | – | – | 100 | mV |
| $g_{fs}$ | forward transconductance | $I_D$ = 8 A; $V_{DS}$ = 10 V | 5 | 7.5 | – | S |
| $g_{fs1}/g_{fs2}$ | forward transconductance ratio of both transistor sections | $I_D$ = 8 A; $V_{DS}$ = 10 V | 0.9 | – | 1.1 | |
| $R_{DS(on)}$ | drain-source on-state resistance | $I_D$ = 8 A; $V_{GS}$ = 10 V | – | 0.1 | 0.15 | Ω |
| $I_{DSX}$ | on-state drain current | $V_{GS}$ = 10 V; $V_{DS}$ = 10 V | – | 37 | – | A |
| $C_{is}$ | input capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 495 | – | pF |
| $C_{os}$ | output capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 340 | – | pF |
| $C_{rs}$ | feedback capacitance | $V_{GS}$ = 0; $V_{DS}$ = 28 V; f = 1 MHz | – | 40 | – | pF |



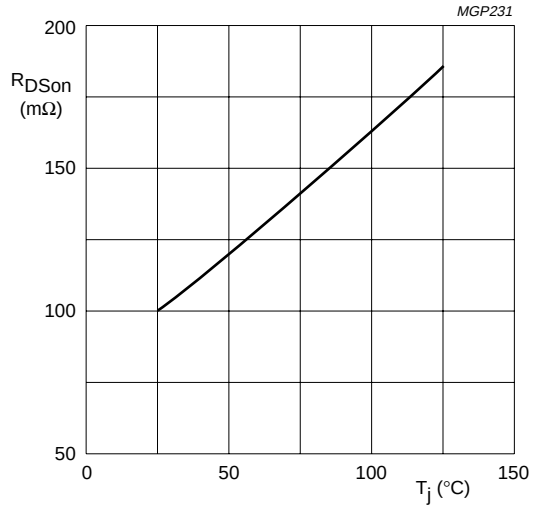

$V_{DS}$ = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



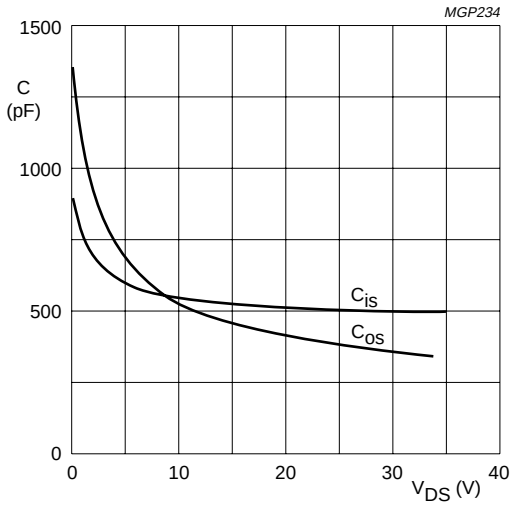

$V_{DS}$ = 10 V; $T_j$ = 25 °C.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



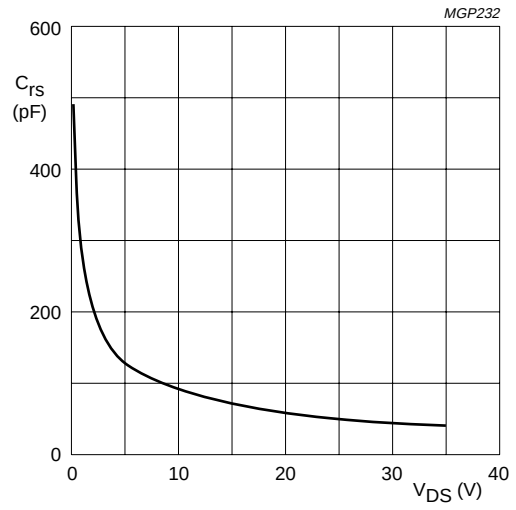

$I_D$ = 8 A; $V_{GS}$ = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.




$V_{GS}$ = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.




$V_{GS}$ = 0; f = 1 MHz.

Fig.8 Feedback capacitance as a function of drain-source voltage, typical values per section.

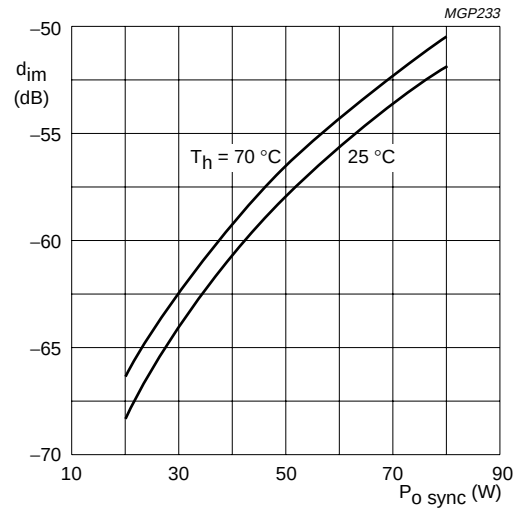



Fig.9 Intermodulation distortion as a function of peak synchronized output power.

## APPLICATION INFORMATION FOR CLASS-A OPERATION

$T_h$ = 70 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W unless otherwise specified.
RF performance in a linear amplifier (common source circuit class-A circuit).
$R_{GS}$ = 82 Ω per section; optimum load impedance per section = 0.14 + j0.14 Ω.

| MODE OF OPERATION | $f_{vision}$ (MHz) | $V_{DS}$ (V) | $I_D$ (A) | $T_h$ (°C) | $d_{im}$ (dB) (note 1) | $P_{o\ sync}$ (W) | $G_p$ (dB) |
|---|---|---|---|---|---|---|---|
| class-A | 224.25 | 28 | 2 × 4.6 | 70 | –52 | > 67<br>typ. 70 | > 11<br>typ. 12.5 |
| | 224.25 | 28 | 2 × 4.6 | 25 | –52 | typ. 75 | typ. 13 |
| | 224.25 | 28 | 2 × 4.6 | 70 | –55 | > 54<br>typ. 57 | > 11<br>typ.12.5 |
| | 224.25 | 28 | 2 × 4.6 | 25 | –55 | typ. 62 | typ. 13 |

**Note**

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak synchronization level.

### Ruggedness in class-A operation

The BLF348 is capable of withstanding a load mismatch corresponding to VSWR = 20 through all phases under the following conditions:

$V_{DS}$ = 28 V; f = 224.25 MHz at rated output power.

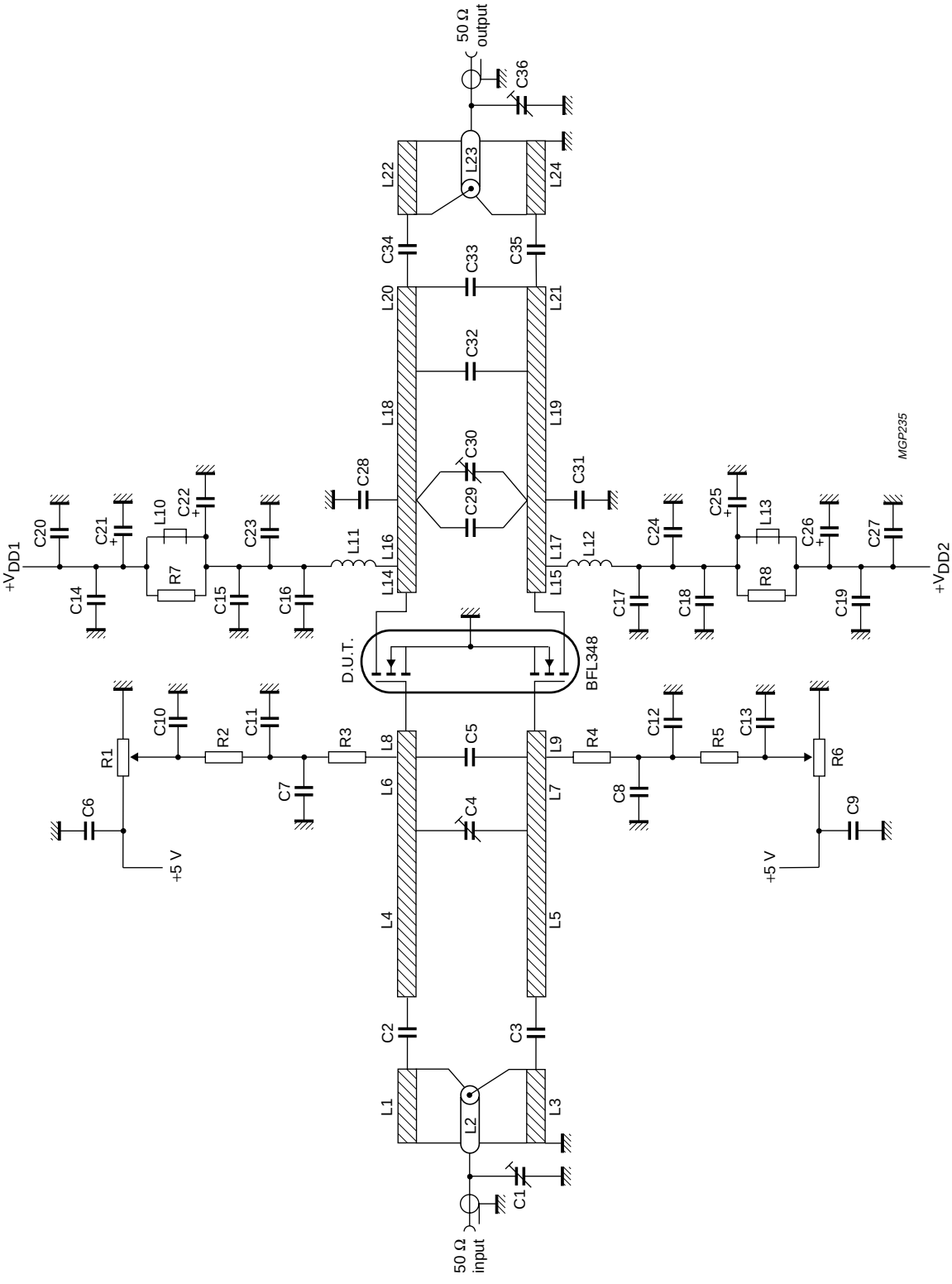



Fig.10 Test circuit for class-A operation.

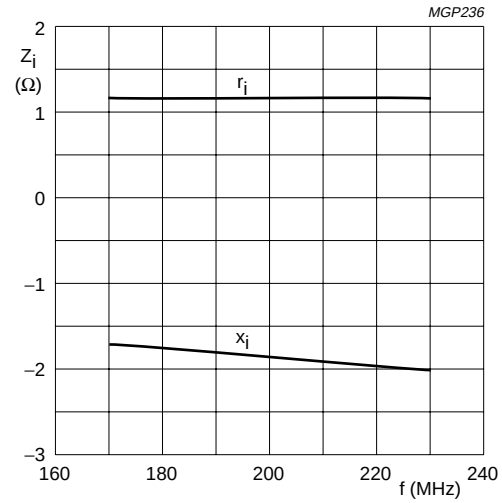
**List of components (class-A test circuit)**

| COMPONENT | DESCRIPTION | VALUE | DIMENSIONS | CATALOGUE NO. |
|---|---|---|---|---|
| C1 | film dielectric trimmer | 2 to 9 pF | | 2222 809 09006 |
| C2, C3 | multilayer ceramic chip capacitor (note 1) | 2 × 10 pF in parallel + 22 pF | | |
| C4, C30 | film dielectric trimmer | 5 to 60 pF | | 2222 809 08003 |
| C5 | multilayer ceramic chip capacitor (note 1) | 82 pF, 500 V | | |
| C6, C9, C10, C13, C14, C19 | multilayer ceramic chip capacitor | 100 nF, 50 V | | 2222 852 47104 |
| C11, C12, C20, C27 | multilayer ceramic chip capacitor (note 1) | 1 nF, 500 V | | |
| C7, C8, C16, C17 | MKT film capacitor | 1 μF | | 2222 371 11105 |
| C21, C26 | electrolytic capacitor | 10 μF, 63 V | | |
| C22, C25 | electrolytic capacitor | 220 μF, 63 V | | |
| C15, C18, C23, C24 | multilayer ceramic chip capacitor (note 1) | 510 pF, 500 V | | |
| C28, C31 | multilayer ceramic chip capacitor (note 1) | 2 × 8.2 pF in parallel, 500 V | | |
| C29 | multilayer ceramic chip capacitor (note 1) | 3 × 39 pF in parallel, 500 V | | |
| C32 | multilayer ceramic chip capacitor (note 1) | 33 pF, 500 V | | |
| C33 | multilayer ceramic chip capacitor (note 1) | 18 pF, 500 V | | |
| C34, C35 | multilayer ceramic chip capacitor (note 1) | 10 pF + 18 pF + 62 pF (3 in parallel), 500 V | | |
| C36 | film dielectric trimmer | 2 to 18 pF | | 2222 809 09003 |
| L1, L3, L22, L24 | stripline (note 2) | 50 Ω | 4.8 × 80 mm | |
| L2, L23 | semi-rigid cable (note 3) | 50 Ω | ext. conductor length 80 mm ext. dia 3.6 mm | |
| L4, L5 | stripline (note 2) | 43 Ω | 6 × 32 mm | |
| L6, L7 | stripline (note 2) | 43 Ω | 6 × 7 mm | |
| L8, L9 | stripline (note 2) | 43 Ω | 6 × 7 mm | |
| L10, L13 | grade 3B Ferroxcube wideband HF choke | 2 in parallel | | 4312 020 36642 |
| L11, L12 | 3/4 turn enamelled 2 mm copper wire | 40 nH | space 1 mm int. dia. 10 mm leads 2 × 7 mm | |
| L14, L15 | stripline (notes 2 and 4) | 43 Ω | 6 × 6 mm | |
| L16, L17 | stripline (notes 2 and 4) | 43 Ω | 6 × 9.5 mm | |
| L18, L19 | stripline (notes 2 and 4) | 43 Ω | 6 × 27.5 mm | |
| L20, L21 | stripline (notes 2 and 4) | 43 Ω | 6 × 13 mm | |

| COMPONENT | DESCRIPTION | VALUE | DIMENSIONS | CATALOGUE NO. |
|---|---|---|---|---|
| R1, R6 | 10 turns Bourns potentiometer | 50 kΩ | | |
| R2, R5 | 0.4 W metal film resistor | 1 kΩ | | |
| R3, R4 | 0.4 W metal film resistor | 82 Ω | | |
| R7, R8 | 1 W, ±5% metal film resistor | 10 Ω | | |

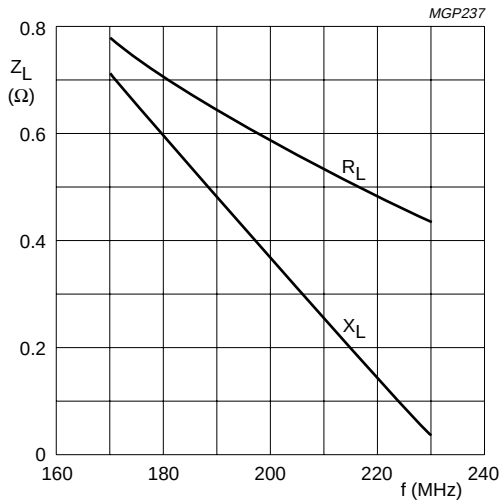
**Notes**

1. American Technical Ceramics (ATC) capacitor, type 100B or other capacitor of the same quality.
2. The striplines L1, L3 - L9, L14 - L22 and L24 are on a double copper-clad printed circuit board with glass microfibre PTFE dielectric ($\varepsilon_r$ = 2.2); thickness $\frac{1}{16}$ inch; thickness of copper sheet 2 x 35 μm.
3. Semi-rigid cables L2 and L23 are soldered on to striplines L1 and L24.
4. A copper strap, thickness 0.8 mm, is soldered on to striplines L14 - L21.



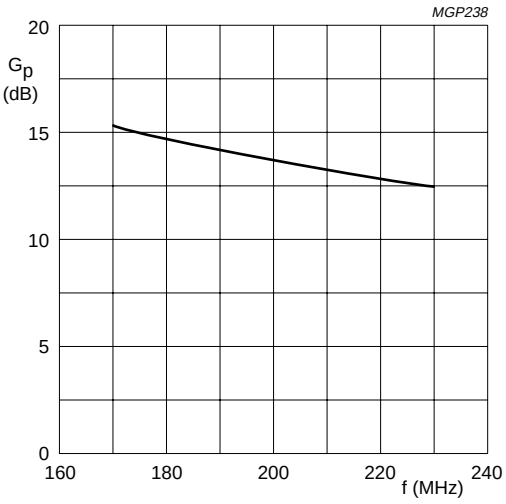

Class-A operation; $V_{DS}$ = 28 V; $I_{DQ} = 2 \times 4.6$ A;
$R_{GS}$ = 82 Ω (per section); $T_h$ = 70 °C.

Fig.11 Input impedance as a function of frequency (series components), typical values.




Class-A operation; $V_{DS}$ = 28 V; $I_{DQ} = 2 \times 4.6$ A;
$R_{GS}$ = 82 Ω (per section); $T_h$ = 70 °C.

Fig.12 Load impedance as a function of frequency (series components), typical values.

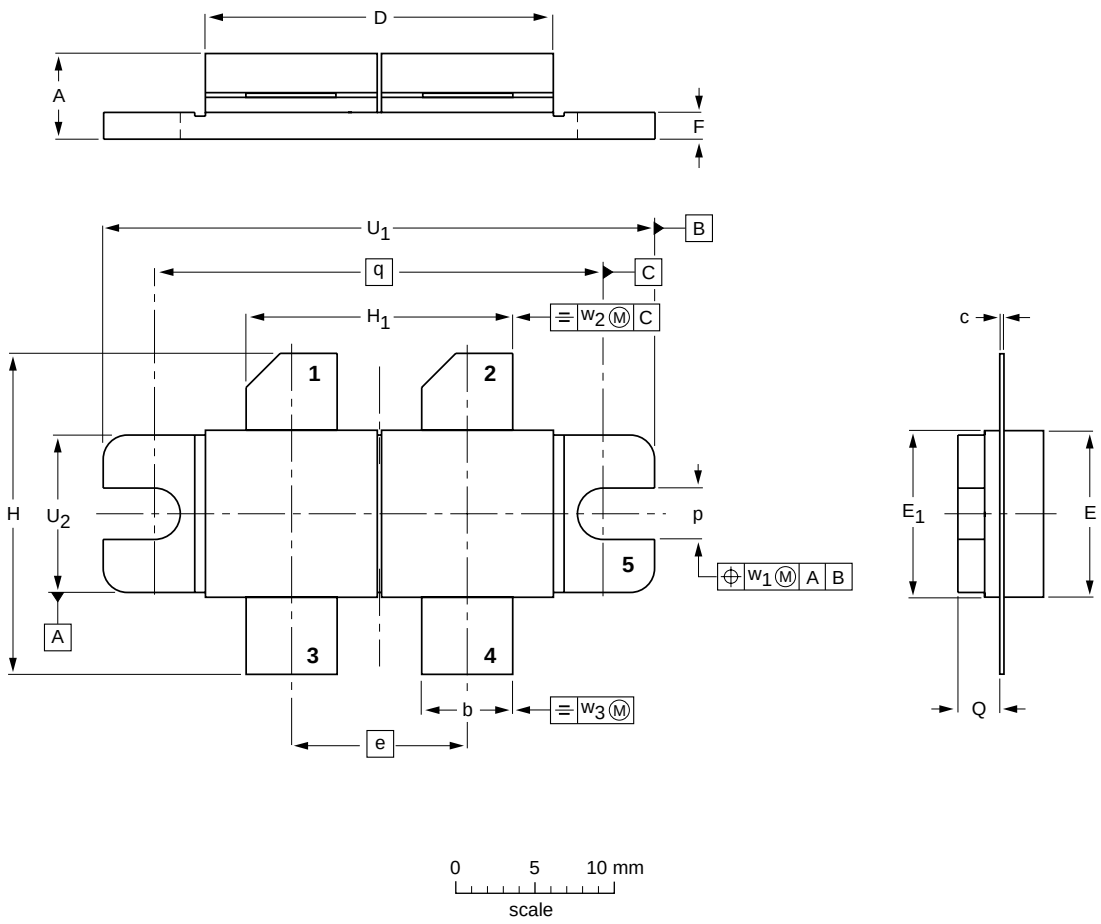



Class-A operation; $V_{DS}$ = 28 V; $I_{DQ} = 2 \times 4.6$ A;
$R_{GS}$ = 82 Ω (per section); $T_h$ = 70 °C.

Fig.13 Power gain as a function of frequency, typical values.

## PACKAGE OUTLINE

**Flanged double-ended ceramic package; 2 mounting holes; 4 leads** **SOT262A1**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

| UNIT | A | b | c | D | e | E | $E_1$ | F | H | $H_1$ | p | Q | q | $U_1$ | $U_2$ | $w_1$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.77<br>5.00 | 5.85<br>5.58 | 0.16<br>0.10 | 21.98<br>21.71 | 11.05 | 10.27<br>10.05 | 10.29<br>10.03 | 1.78<br>1.52 | 20.58<br>20.06 | 17.02<br>16.51 | 3.28<br>3.02 | 2.85<br>2.59 | 27.94 | 34.17<br>33.90 | 9.91<br>9.65 | 0.51 | 1.02 | 0.25 |
| inches | 0.227<br>0.197 | 0.230<br>0.220 | 0.006<br>0.004 | 0.865<br>0.855 | 0.435 | 0.404<br>0.396 | 0.405<br>0.395 | 0.070<br>0.060 | 0.81<br>0.79 | 0.67<br>0.65 | 0.129<br>0.119 | 0.112<br>0.102 | 1.100 | 1.345<br>1.335 | 0.390<br>0.380 | 0.02 | 0.04 | 0.01 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT262A1 | | | | | | 97-06-28 |

**DEFINITIONS**

| **Data Sheet Status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

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